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Charge trapping in a double quantum well system

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Abstract

The effect of charge trapping in a double quantum well system is studied by undertaking transport measurements at 1.2 K as a function of front gate voltage. On sweeping the gate bias between −0.2 and 0.6 V, the trapping of electrons in the defect levels induced by the AlGaAs barrier is complemented by the decrease in the overall carrier density in the quantum well. The charging of these defect levels increases the scattering potential and enhances the overall resistance of the two dimensional electron gas. The trapped charges were completely depleted on reverse sweeping the gate bias to −0.1 V. The charging and discharging of the defect levels gave rise to a hysteresis effect in the transport measurements.

1. Introduction

A double quantum well system (DQW) comprising two dimensional electron gases (2DEG) in parallel is a versatile structure for the fabrication of quantum electric and optical devices such as a double layer electron transistor [1], magnetic resonant tunneling diodes [2], a quantum well infrared detector [3], and a double barrier terahertz source [4]. During the growth process of all these devices, defect centers are induced between the conduction and valence band due to the lattice relaxation process which act as electron traps [5, 6]. These defects and traps affects the fundamental device characteristics such as mobility, carrier density, saturation current, optical emission efficiency and emission wavelength [7–10]. Apart from this, the traps are known to be responsible for the persistent photoconductivity effect [11].

During the room temperature operation of the quantum well devices the traps will contribute to the dark currents which hamper the efficiency of quantum optical devices making the room temperature operation extremely challenging [12]. Moreover the traps also destroy the translational invariance necessary for the successful operation of tunneling devices [13]. Most of the previous studies on the charge traps were mainly related to the defects induced by strain relaxation during the growth process of self-assembled InAs quantum dots [14–16]. To date there is scarcely any detailed report on the defect related centers that exist at the GaAs/AlGaAs interface. Considering the high concentration of AlGaAs defects normally encountered in high electron mobility transistors (HEMTs) it will be of interest to study the effects of these defect induced traps on the transport properties of the 2DEG in the double quantum well system [17]. Since it is difficult to isolate the effect of traps on the electron dynamics at room temperature due to the dominating effect of phonons under such conditions, the present work is carried out at low temperature by employing four terminal magnetoresistance measurements.

2. Experiment

The sample used for this study consists of two GaAs quantum wells each of width 180 Å separated by a 100 Å AlGaAs barrier and, is grown on a GaAs substrate by molecular beam epitaxy (figure 1). The electrons were provided by the Si doping (n^+) layer on each side of the quantum wells with a doping density of 1.1×10^{17} cm^{-3}. The doping layers were separated from the quantum wells by AlGaAs layers with a thickness of 400 Å to reduce the broadening effect due to ionized impurity potential. The carrier densities in the quantum wells were controlled using the front gate (V_g). Four terminal magnetoresistance measurements were taken using the standard lock-in detection

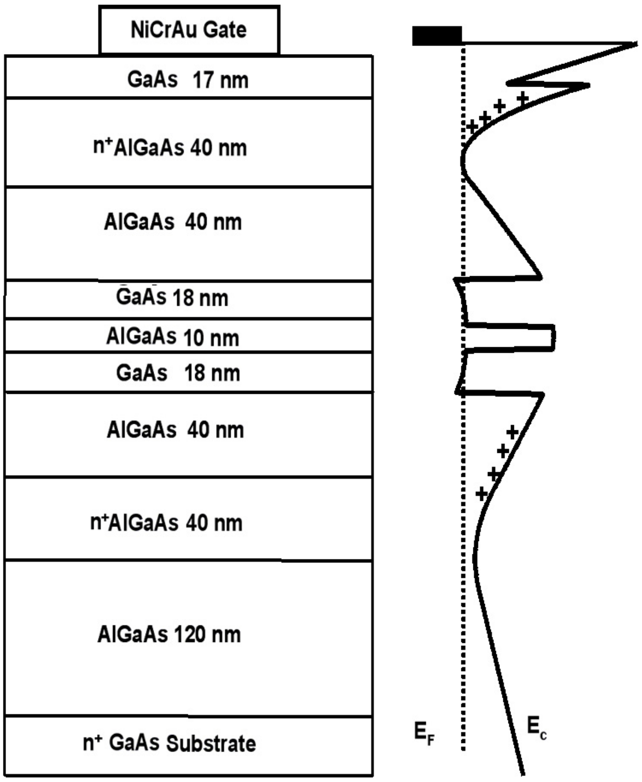

Figure 1. Structure and conduction band diagram of the sample.

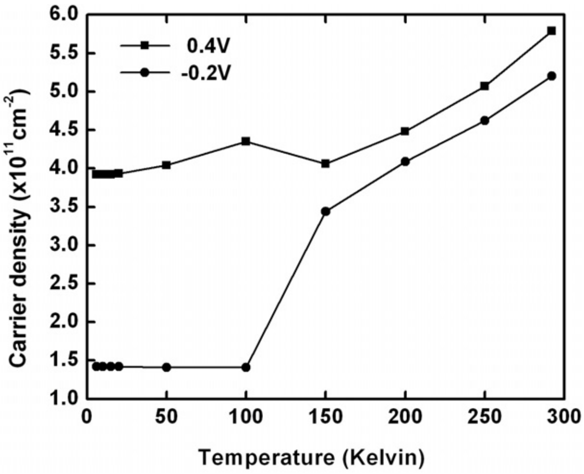

Figure 2. Variation of carrier density with temperature corresponding to $V_g = -0.2$ and 0.4 V.

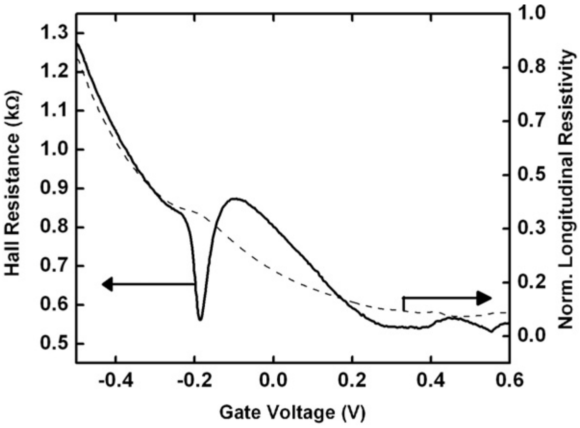

Figure 3. Variation of zero field longitudinal resistivity and Hall resistance at 0.3 T as a function of gate voltage in sample A.

technique by applying magnetic field perpendicular to the 2DEG in a liquid helium cooled cryostat.

3. Results and discussion

In figure 2, the variations in the total carrier density of the DQW is plotted as a function of temperature for $V_g = -0.2$ and 0.4 V. For $T > 150$ K, no appreciable difference in the carrier density is observed between the two gate voltages. In this temperature range, the carrier density in the quantum well is highly sensitive to temperature fluctuations due to the excitation of carriers from the valence to the conduction band and the gate bias has little control over the carrier density in the quantum well. On decreasing the temperature below 150 K, the carrier density abruptly drops for $V_g = -0.2$ V and thereafter remains constant. This indicates that there is a negligible amount of carrier excitation from the valence band to the conduction band. Moreover at -0.2 V the traps are in a completely depleted state as their electronic levels are lifted off above the Fermi level and hence there will be no contribution from them at this value of V_g. For $V_g = 0.4$ V, the carrier density does not show any significant change as the temperature is decreased from 150 to 6 K. This behavior might be due to the excitation of carriers from the valence band and the traps whose electronic level is now below the Fermi level due to the positive bias applied to the gate. The sample is then further cooled to 1.2 K so that any thermal excitation of electrons to the conduction band is completely frozen out. At this temperature the only possible contribution towards the change in the carrier density of the quantum well must come from the tunneling of electrons between the conduction band and the traps [18]. This carrier capture by the traps from the quantum well will have an effect on the behavior of the longitudinal and Hall resistance measurement.

To investigate this behavior, the variation in the longitudinal resistivity (ρ_{xx}) and Hall resistance (ρ_{xy}) at 0.3 T is plotted as a function of gate voltage at 1.2 K (figure 3). When the gate bias (V_g) is at -0.5 V, the upper well is completely depleted and the carriers are confined only in the lower quantum well. The current in this regime flows only through the lower 2DEG. On increasing V_g gradually, the value of ρ_{xx} is found to decrease due to the enhancement in the screening effect of the 2DEG with increasing carrier density. At -0.2 V, electrons begin to populate the upper well. At this instance the presence of electrons in the two quantum wells contribute to interlayer electron interaction and a small plateau is observed in the ρ_{xx} trace [19]. Simultaneously the Hall voltage across both the layers will be forced to be identical as the 2DEGs are shorted together at the ohmic contacts. Therefore to maintain equilibrium in each layer, the proportion of the current passing through each layer is altered which causes a sudden drop in the current flowing through the lower 2DEG [20]. The sudden drop in the current in the lower quantum well induces a sharp decrease in ρ_{xy} at −0.2 V as observed in figure 3. Once the Hall voltage attains equilibrium in both conducting channel, the net current increases again to its original value and the Hall resistance shows a sharp increase. If independent contacts were made to the 2DEGs, the two conducting layers develop different Hall voltages and no such effects will be observed.

On further increasing V_g, a sudden increase in the ρ_{xy} is observed at 0.42 V. This is unexpected given that the density of the 2DEG is increasing continuously. On repeating the measurement several times, the same feature is consistently observed. This increase in ρ_{xy} implies a slight decrease in the carrier density of the quantum well as the ρ_{xy} is an inverse function of carrier density ($\rho_{xy} = B/n_s e$), its value is likely to increase with the decrease in the carrier density of the 2DEG. In addition to this, a small kink in ρ_{xx} is also observed at this value of V_g. It is a well established fact that the increase in ρ_{xx} indicates enhancement in the scattering potential experienced by the 2DEG. To better understand the physical mechanism for this behavior, V_g is cyclically ramped between −0.2 and 0.6 V and the variation in carrier densities of the quantum wells and ρ_{xx} is determined as a function of gate voltage.

It is to be noted that as the gate voltage becomes more positive only the carrier density in the upper well will undergo changes with V_g and no changes will take place in the lower quantum well, as the lower 2DEG is immune to the changes in V_g due to the screening effect of the upper 2DEG [21]. If any change is observed in the total carrier density, it must be due to the depletion of some of the carriers in the upper quantum well.

The change in the carrier density is then identified from the shift in the Fourier peaks during the forward and reverse sweep. The individual carrier densities for the upper and lower quantum well are calculated by Fourier transforming the Shubnikov–de Hass (SdH) oscillation. Previously from the behavior of ρ_{xx} and ρ_{xy} (figure 3), it was speculated that the abrupt increase in their values at 0.42 V is due to the tunneling of carriers from the quantum well into the charge traps. The electrons once captured will only be depleted by applying a negative bias to the gate. Therefore considering the scenario that some of the electrons that tunnel into the traps at 0.42 V are depleted only for $V_g < 0$, it is expected that for $0 \text{ V} < V_g < 0.44$ V, the carrier density peak of the upper well corresponding to forward and reverse sweep must show a shift in the Fourier spectrum. From the shift, the number of electrons that have tunneled into the traps can be ascertained. This behavior is clearly observed from the Fourier power spectrum corresponding to 0.3 V shown in figure 4. From the plot, the difference in the carrier density is found to be approximately 0.54×10^{11} cm^{-2}. The values calculated for all the other gate voltages between 0 and 0.44 V was found to be consistent within reasonable accuracy.

The other possible mechanism for the electrons to get depleted from the quantum well when V_g is increasing is by exchange interaction between the quantum wells. The possibility of exchange interaction is very remote considering the fact that such a phenomenon takes place at very low carrier densities. Moreover in exchange interaction assisted charge transfer the total carrier density remains the same, which is not the case observed here. Therefore the most likely scenario is that the electrons from the quantum well are trapped in the energy levels of the defect states that are inherently present in our sample. The electrons tunnel into these traps on applying a positive bias as the energy level of the conduction band is pulled down. This will in turn reduce the energy difference between the bottom of the conduction band and the energy level of the defects present in the band gap creating a favorable condition for the electrons in the 2DEG to tunnel into the defect levels. Moreover this charged trap level contributes to scattering potential and increases ρ_{xx} which accounts for the kink observed in our measurement. For $V_g > 0.42$ V, the charge traps are already saturated with electrons and no further transfer of charges are takes place. This is also evident from the Fourier spectrum taken at 0.6 V in which the carrier density peaks corresponding to upper and lower quantum well in the forward and reverse sweep almost coincide with each other (figure 4).

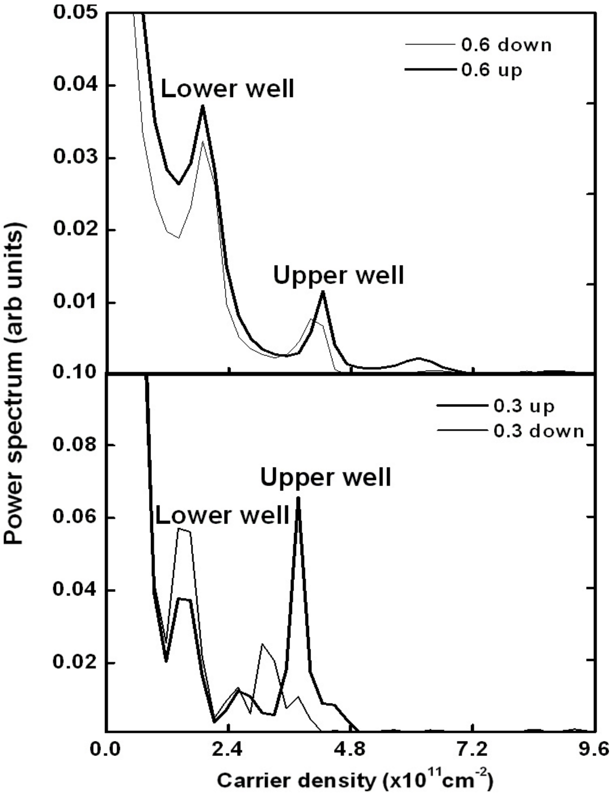

Figure 4. Fourier spectrum of SdH oscillation for sample A at 0.6 and 0.3 V.

The charge trapping is confirmed from the hysteresis observed in the ρ_{xx} trace as shown in figure 5. The ρ_{xx} trace corresponding to the forward and the reverse sweeps traverses different paths for $-0.1 \text{ V} < V_g < 0.42$ V. For $V_g < -0.1$ V, the trapped charges are completely depleted and the two resistance traces merge with each other. Hence by switching the gate voltage between 0.6 and −0.1 V the

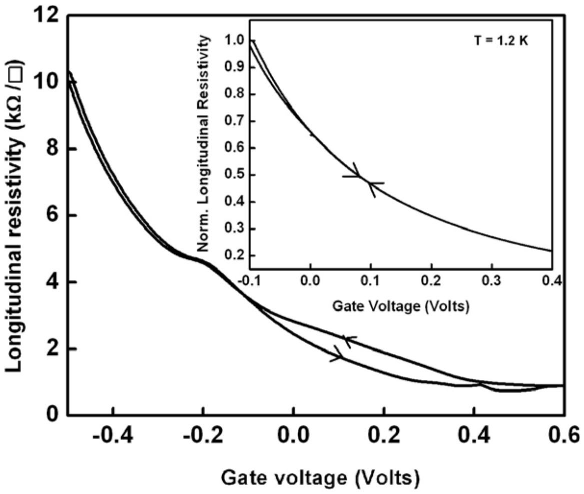

Figure 5. Hysteresis effect in the double quantum well sample at 1.2 K. Inset: normalized longitudinal resistivity as a function of gate voltage.

traps can be charged and discharged with electrons. Since the electrons are trapped only when V_g becomes 0.42 V, no hysteresis is expected if the value of V_g is kept below this threshold limit. This expected behavior was observed and no hysteresis characteristics show up when the gate bias is swept forward and backwards between −0.1 and 0.4 V (inset to figure 5).

4. Conclusion

From our detailed study it is clear that the presence of traps has a profound effect on the transport properties of the quantum well based devices at low temperature and contributes to significant dark current at room temperature. Apart from acting as scattering centers these traps also induce hysteresis in the resistance measurements. Such hysteresis effects due to traps are undesirable for quantum well based electrical devices. However the trap induced effects can be significantly reduced by operating the devices below the threshold voltage limits which happens to be 0.42 V in the present case. In this way the performance of quantum devices can be made more reliable and their performance can be optimized.

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